

**REMARKS**

Examiner Thomas L. Dickey is thanked for his examination of the subject Patent Application. The Specification, Drawings and Claims have been carefully reviewed with respect to the cited prior art, a substitute drawing has been formed, the Claims have been amended and are considered to be in condition for Allowance.

**Claim Status**

Claims 1-3, 5 and 6 remain in this application.

**Detailed Action Item 1 & 2****Drawings**

The Applicant acknowledges the approval of substitute drawings filed on 07/31/02 together with the amendment to the specification referring to those drawings.

**Additional Drawing Corrections**

However, upon further review of the FIG. 2m, the Applicant urges that this drawing be replaced by a substitute drawing (FIG. 2m) as being a much improved rendition of the original specification and claims. This is discussed below in reference to the cited prior art.

**Detailed Action Item 3****Claim Rejections - 35 USC § 102(e)**

Reconsideration of the rejection of Claim 1 under 35 U.S.C. 102(e) as being anticipated by CHANG (US 20010045594) is requested based on the

following arguments.

The Examiner's described one of Chang's illustration as being similar to the previously amended Claim 1. It is believed that the Examiner is referring to Chang's FIG. 3 showing prior and not Chang's FIG.4 which is a top view of his invention, and the Applicant's response is directed to FIG. 3. FIG. 3 fits the description, FIG. 4 does not.

The instant Claim 1 has been amended to clearly describe a floating gate structure having extent and shape as seen in original FIGs. 2k, 2l, and 2m but not as shown in Chang's FIG. 3. The instant floating gate structure has a body length which is limited to act as a mask to define and implant source and drain regions 200 as illustrated in FIG 2l. Therefore the floating gate structure is contained within the active area which also aids in conserving substrate real estate. This is in contrast to the shape of the prior art floating gate 16 which extends beyond the active are and which is not used as a mask for implantation into the region below the gate oxide 12 area. Apparently that prior art implantation takes place prior to forming floating gate 16. However, another disclosure attributable to Chang as found in FIGs. 5B, 5C, 5D and 5E does show a gate structure 52 that is limited in length and is used as a mask for implantation of source and drain areas 58. But this gate structure 52 as shown in FIG. 5E particularly in the region of the second gate oxide 56 is a simple flat surface that is replicated at reference numerals 56, 68 and the control gate polysilicon 70 as flat surfaces. Contrary to Chang's floating gate, the instant floating gate has a multiply connected top surface and it is that shape that is replicated conformally in

the inter-poly dielectric 170 and into the control gate 180 as shown in original FIGs. 2j, 2k, 2l and 2m.

The instant specification at page 14, line 20 reads as follows:

"It will be observed that the surface of the first polysilicon layer exposed in (125) can "folded" several time over by having several steps or "fins" similar to that is found in heat sinks. Furthermore, the fins can comprise other shapes , such as triangular, or trapezoidal, and so on, all designed to increase the surface area."

and original claim 4 further listed rectangular shapes. It should be noted that these shapes that define the multiply connected floating gate surface are found within the floating gate body which is limited in length to serve as a mask. That is to say these shapes are part of that "masking" floating gate and are designed within the active area.

Referring back to FIG. 3 of Chang, the floating gate 16 does not have rectangular, triangular or trapezoidal shapes defining the top surface. The floating gate 16 can be described as a gull wing over its extent or as having a horizontal surface and two sloped surfaces over the projected active area. Or it could be described as having a bottom and a top surface that are replications of the top surface of the thin gate oxide over the active area flanked by the thick field oxides beyond the active area.

The drawing, FIG. 2m, which was approved on 07/31/02 indeed shows a floating gate body 120 overlying the active area consisting of a multitude of triangles 205 that are replicated into the control gate 180.

Claim 1 has been amended to clearly describe the instant floating gate structure as discussed above. In brief, the instant floating gate structure body is

limited over the active area, it has multiple of triangular, rectangular or trapezoidal cross-sectional shapes within that body such that the resulting top surface area is multiply connected and significantly greater than the area of the bottom surface which is contained within the active area.

#### **Amended Drawing**

Recently approved FIG. 2m has been reviewed and it is now felt that it may be confusing and thus fail to clearly illustrate the invention. To this point, original FIG. 2m shows a multitude of very small triangular cross-sectional shapes that may be perceived as depicting a "rough" top surface the floating gate 120 that is replicated into a "rough" bottom surface of the control gate 180 via a very "thick" inter-poly dielectric 170 which would appear to contribute very little to a designed "increase in the surface area" for increased coupling reasons leaving only the left and right larger sloped regions to provide for that increase. Furthermore, the median thickness of the floating gate is 2000 Å, the depth of the cross-sectional shapes is approximately 1000 Å and the inter-poly dielectric thickness is about 200 Å as respectively claimed in Claims 2, 3 and 5. These proportions need to be illustrated. For the above reasons a substitute figure, FIG. 2m is submitted. No amendment to the specification is needed to be made relative to this substitution.

#### **Detailed Action Item 4**

#### **Claim Rejections - 35 USC § 103**

Reconsideration of the rejection of Claim 5 under 35 U.S.C. 102(e) as

being unpatentable over CHANG (US 20010045594) in view of FUKUMOTO et al. (20020096704) is requested based on the following arguments.

The Applicant believes that the Examiner to mean that Chang does not provide an inter-poly dielectric as an ONO which is 15-25 nm. Thick. Chang uses other than ONO and does not mention thickness. With this understanding the Applicant agrees with the Examiner.

Referring to Fukumoto, it is seen that the inter-poly dielectric layer 5 comprises ONO which is 15 nm thick as shown in FIGs. 10 and 11 and paragraph 15 as observed by the Examiner. However, FIGs 13-18 are more illustrative of the difference in the instant use of ONO at the claimed thickness. Noted in all figures is a floating gate 4 that has a simple shape, a flat top surface similar to that of Chang's floating gate 54 as discussed above. The important difference between the instant inter-poly dielectric and that of Fukumoto is not in the use of ONO, but in the appropriate thickness required by the Applicant to assure optimal insulation thickness that can replicate the floating gate top surface faithfully into the bottom surface of the control gate 180. In that respect the Applicant believes Claim 5 is novel despite it also being dependent on independent Claim 1.

#### **Detailed Action Item 5**

#### **Response to Arguments**

The Applicant agrees with the Examiner that Chang does not show a floating gate that is entirely flat. The claims have been amended to distinguish the instant floating gate from the newly presented prior art.

### CONCLUSION

We have reviewed the related art references made of record and agree with Examiner Dickey that none of these suggest the present claimed invention.

In light of the above arguments and improved drawings, it is suggested that the Claims now clearly describes the invention. All claims are therefore believed to be in condition for allowance.

Allowance of all claims is therefore respectfully requested.

It is requested that should Examiner Dickey not find that the Claims are now Allowable that the Examiner call the undersigned attorney at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'SBA', written in a cursive style.

Stephen B Ackerman, Reg. No. 37,761

## Appendix

## MARKED UP CLAIMS

1. (CURRENTLY AMENDED) A stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of [different] individual shapes comprising:

a semiconductor substrate having an active area;

[a floating Poly-Si gate with multiply connected surfaces having regions of different cross-sectional shapes, said Poly-Si gate having a flat bottom surface;]

a floating Poly-Si gate with a bottom surface and a multiply connected top surface;

said bottom surface being flat and overlying said active area;

said multiply connected top surface overlying said bottom surface; said multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of said multiply connected top surface overlying said active area is greater than the area of said bottom surface;

wherein said individual cross-sectional shapes are selected from a group consisting of rectangular, trapezoidal and triangular shapes;

a conformal inter-poly dielectric layer replicating said individual cross-sectional shapes over said floating Poly-Si gate; and

a conformal Poly-Si control gate replicating said individual cross-sectional shapes over said inter-poly dielectric layer.

2. (ORIGINAL)                      A stacked-gate flash memory cell of claim 1, wherein said floating Poly-Si gate has a thickness between about 1900 to 2100 Å.

3. (CURRENTLY AMENDED)      A stacked-gate flash memory cell of claim 1, wherein said regions of [different] individual cross-sectional shapes have a depth between about 900 to 1000 Å.

4. (CANCELLED)

5. (ORIGINAL)                      A stacked-gate flash memory cell of claim 1, wherein said inter-poly dielectric layer is oxide-nitride-oxide having a thickness between about 150 to 250 Å.

6. (ORIGINAL)                      A stacked-gate flash memory cell of claim 1, wherein said Poly-Si control gate has a thickness between about 1500 to 2000 Å.